

Control Gate-Bit Line Leakage induced Cobalt Silicide Migration in 0.15um Embedded Flash Memory Devices

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Of late, the flash device market has been growing at a rapid pace. During mass production, we often encounter the process variation in terms of film thickness, lithography and etch critical dimensions, from which the following issues of flash cell functionality, yield and reliability arise. Moreover, as the embedded flash memory device contains many high voltage related circuitries, the consequently arising high voltage stress often causes unexpected phenomenon via localized physical damages. This paper, therefore, will be focusing on abnormal phenomenon induced by electrical stress during operations in our 0.15um embedded flash devices.

For programming and erase, high voltage is supplied to the control gate or bit line contact in embedded flash devices. When the threshold voltage (V_t) window is lower than expected due to process variation, trimming is required to enhance the cell performance in the embedded flash device, and in order to support enough voltage for trimming, the charge pump should be able to generate high voltage. In our 0.15um flash memory devices one of the critical yield failures is a control gate-bit line leakage. Failure analysis (FA) using Transmission Electron Microscopy (TEM) shows a lack of Co silicide, which should have been found at the top of the control gate for contact. In our flash device the original voltage applied to the control gate was 10V for programming.

In order to simulate missing Co silicide phenomenon using high voltage stress, we selected Co silicided poly resistor, applying high voltage (15V) to the Co silicided poly resistor via contact. During the electrical stress, current suddenly dropped and sheet resistance jumped up to 500ohm/sq from 10ohm/sq at around 4.6sec stressing (Fig. 1). From Failure Analysis (Fig. 2), it was found that not only was the missing Co silicide discovered near the contact plug and unusually thick polysilicon of 2750Å as compared to normal silicided poly resistor (1750Å) was also discovered there. Before the Co-silicide reaction, the deposited poly silicon thickness was 2000Å. After further experiments, it was confirmed that electrical stress causes Co silicide migration and there is also a critical stress density to trigger this migration.

For the first time, we will report the possible mechanism of Co silicide migration induced by the electrical stress which results from control gate-bit line leakage in our 0.15um embedded flash memory device.

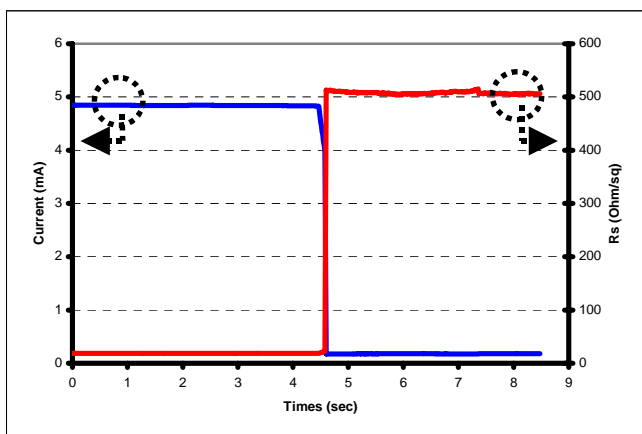


Fig. 1. Current and Sheet resistance with constant voltage stress (15V) as a function of time at Co silicided poly resistor

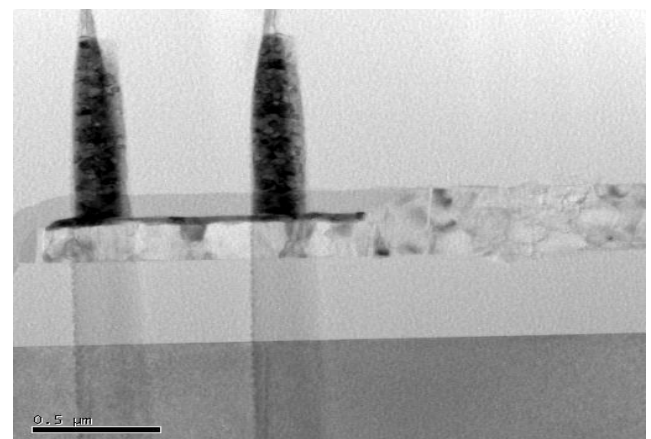


Fig. 2. Missing Co silicide area on poly resistor after electrical stress